EE 505

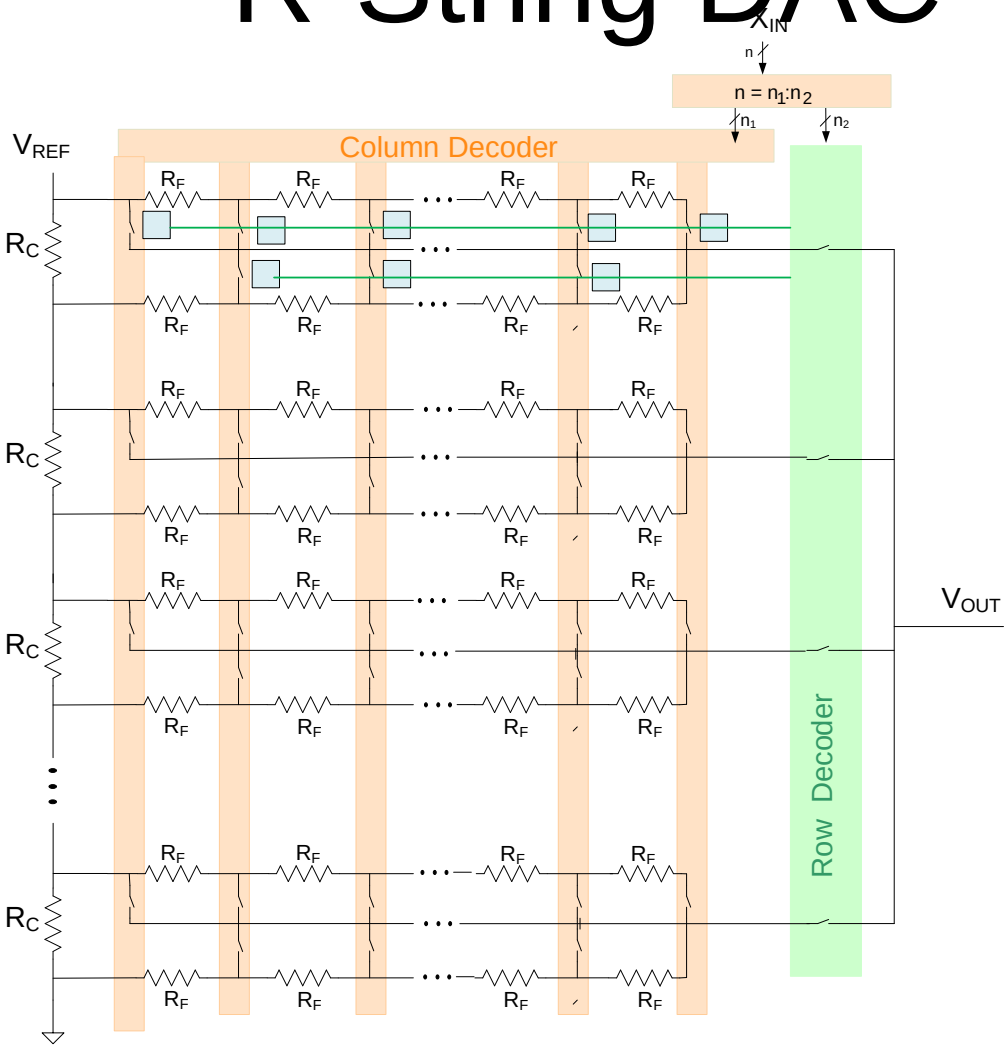
Lecture 15

String DACs

Current Steering DACs

Review from Last Lecture

R-String DAC



Note Dual Ladder is used !

: AND pixel sensor gate

32x32 Matrix

A 10-b 50-MHz **CMOS D/A** converter with 75-ω buffer

MJM **Pelgrom** - Solid-State Circuits, IEEE Journal of, 1990 - ieeexplore.ieee.org

Abstracf-A 10-b 50-MHz digital-to-analog (D/A) converter is pre-sented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, ...

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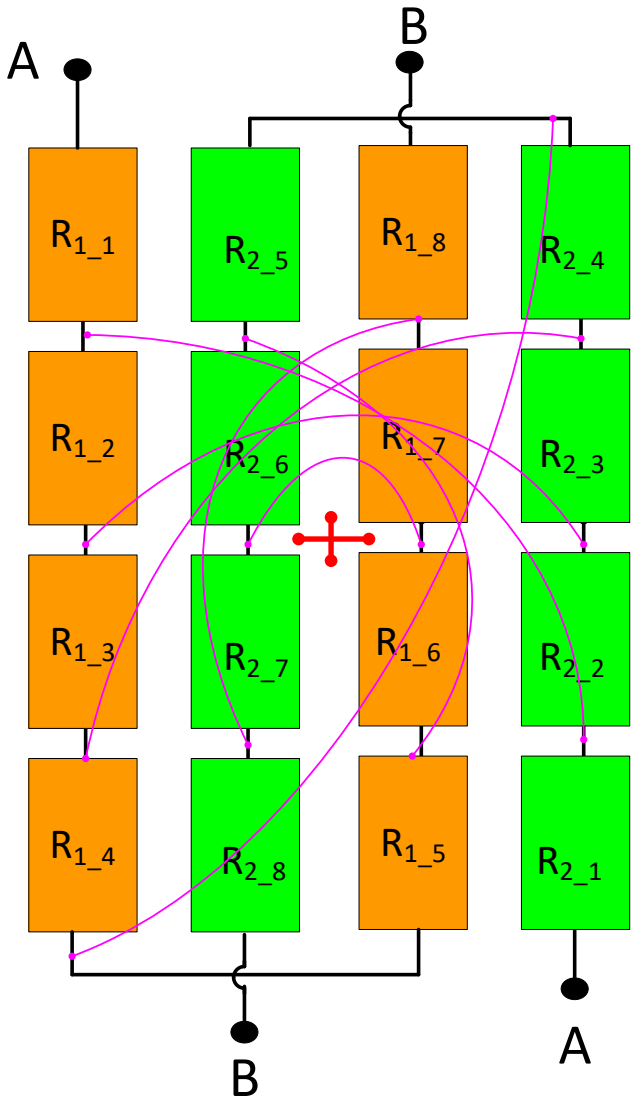
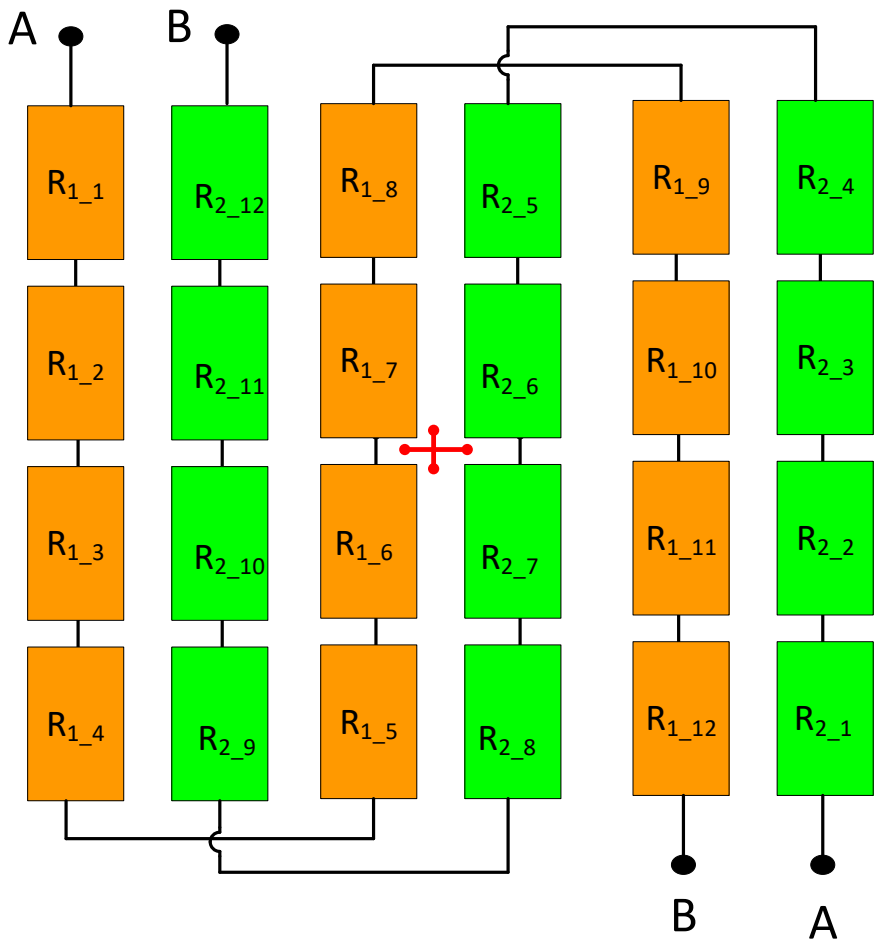
Review from Last Lecture

Common-Centroid Anti-Parallel Ladder Layout



Review from Last Lecture

Common-Centroid Anti-Parallel Ladder Layout

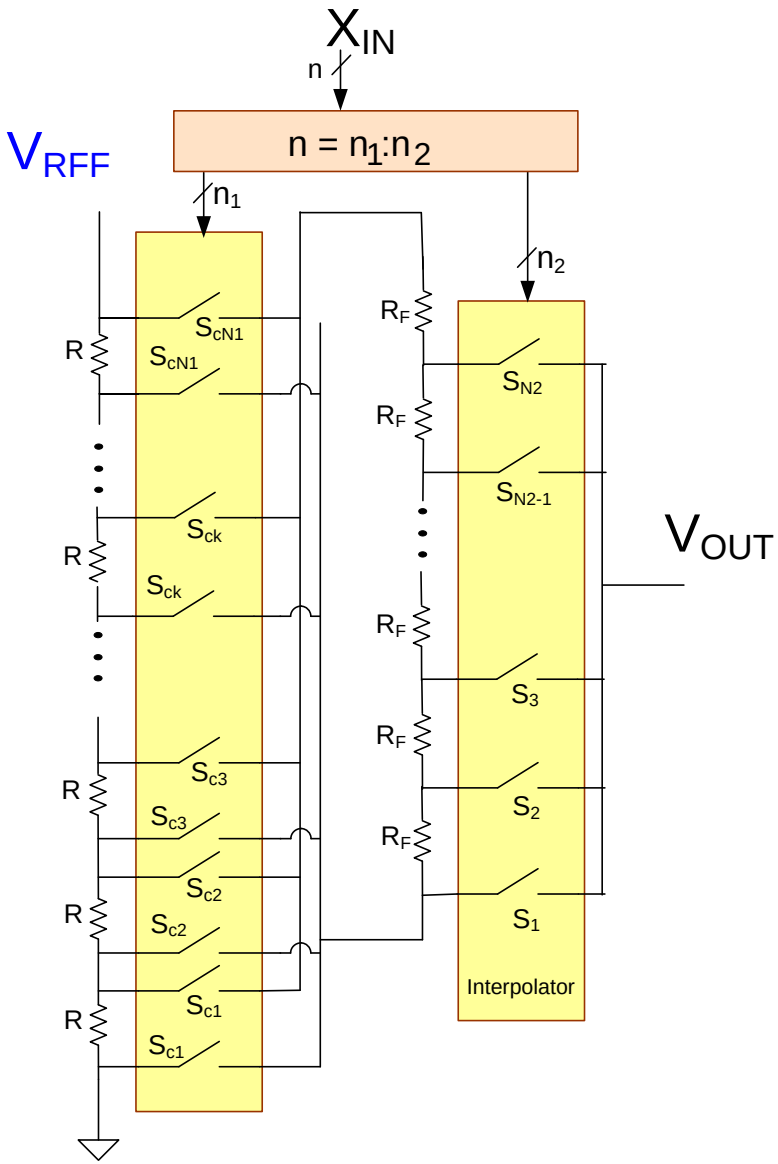


Interconnects Not Shown

Review from Last Lecture

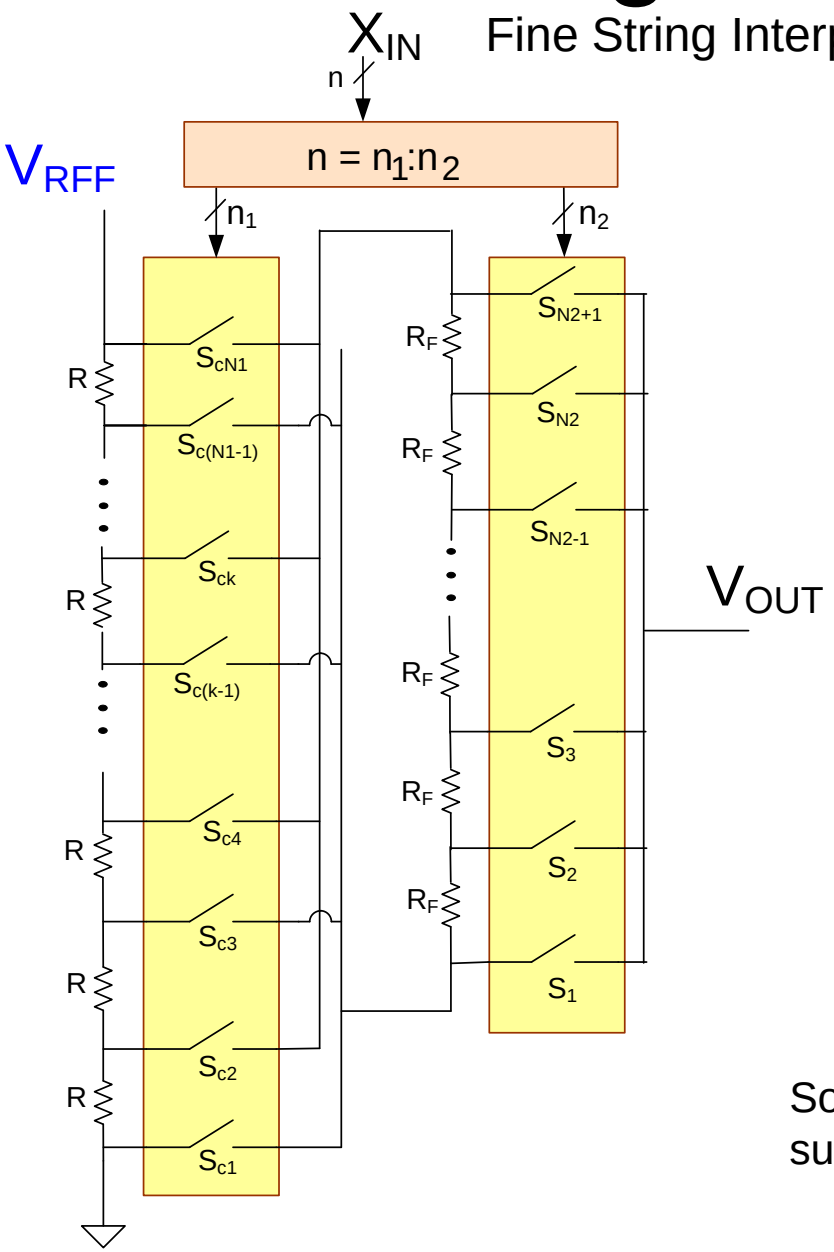
R-String DAC

Fine String Interpolator



Review from Last Lecture

R-String DAC

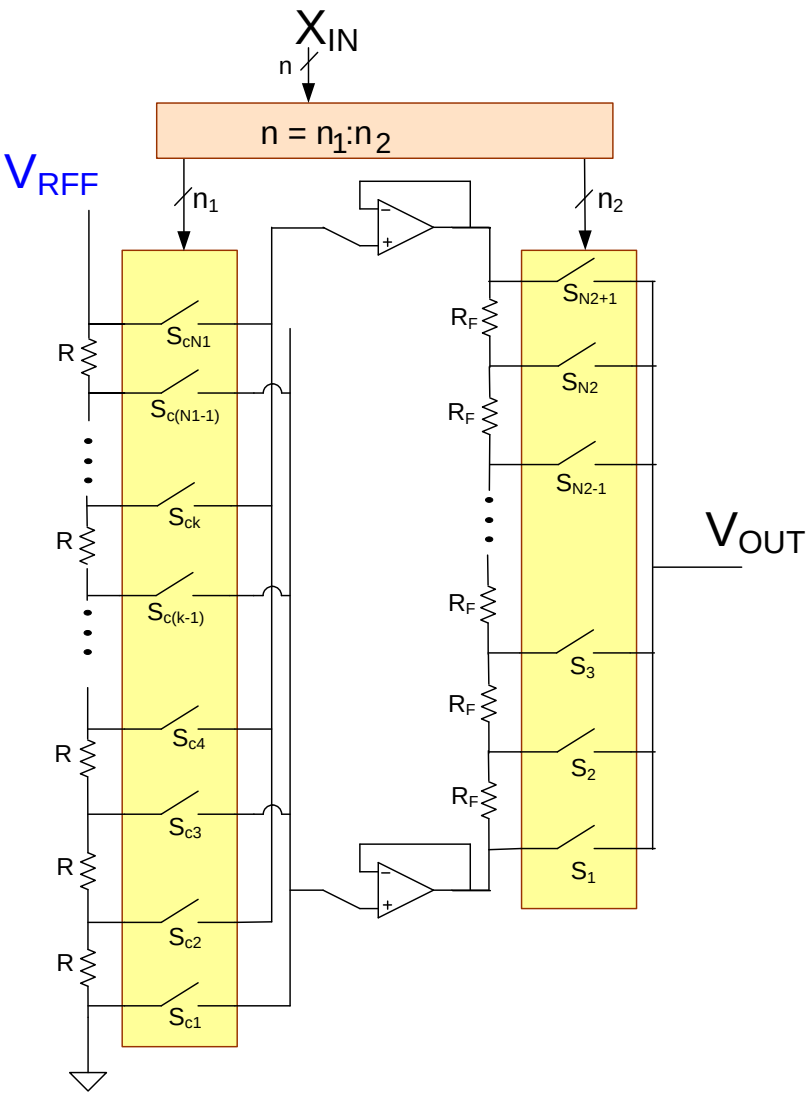


Sometimes termed sub-divider, sub-range or dual-string DAC

Review from Last Lecture

R-String DAC

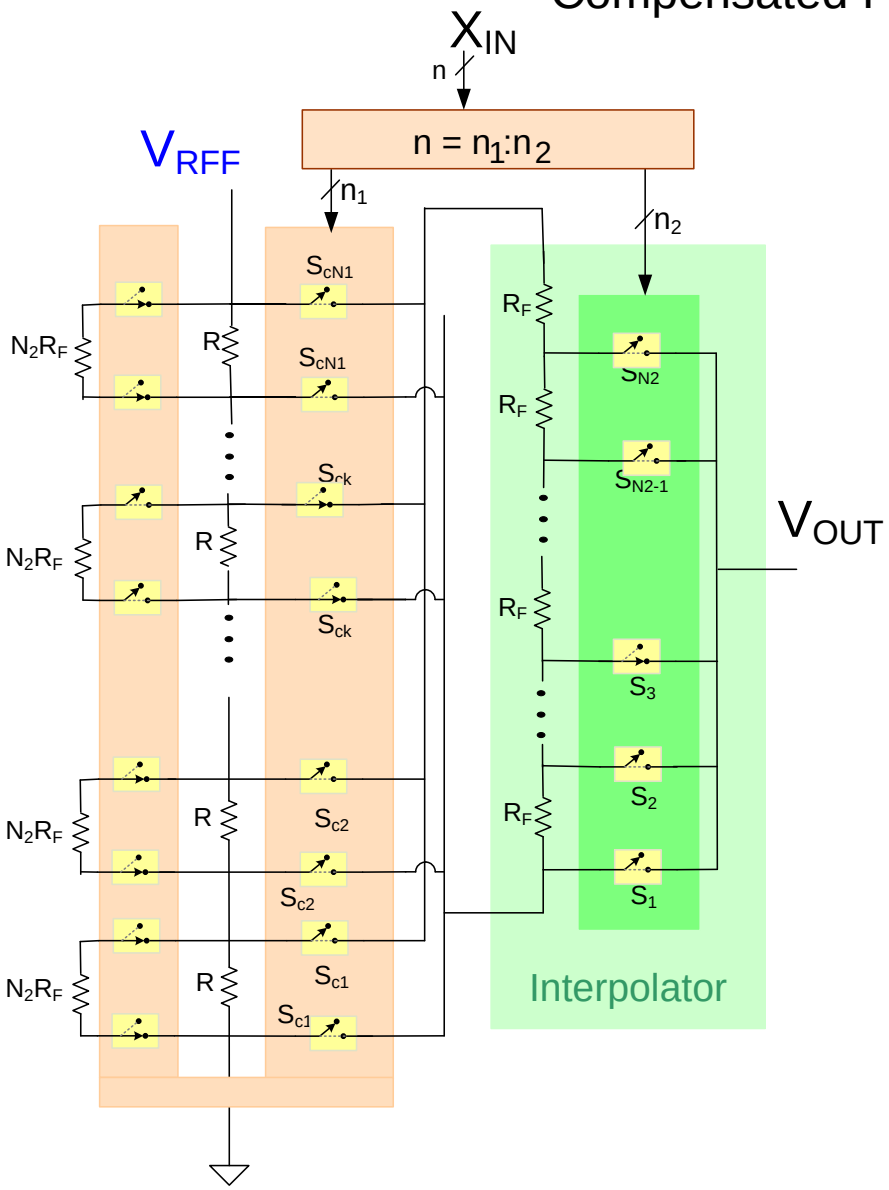
Buffered Fine String Interpolator



Review from Last Lecture

R-String DAC

Compensated Fine String Interpolator



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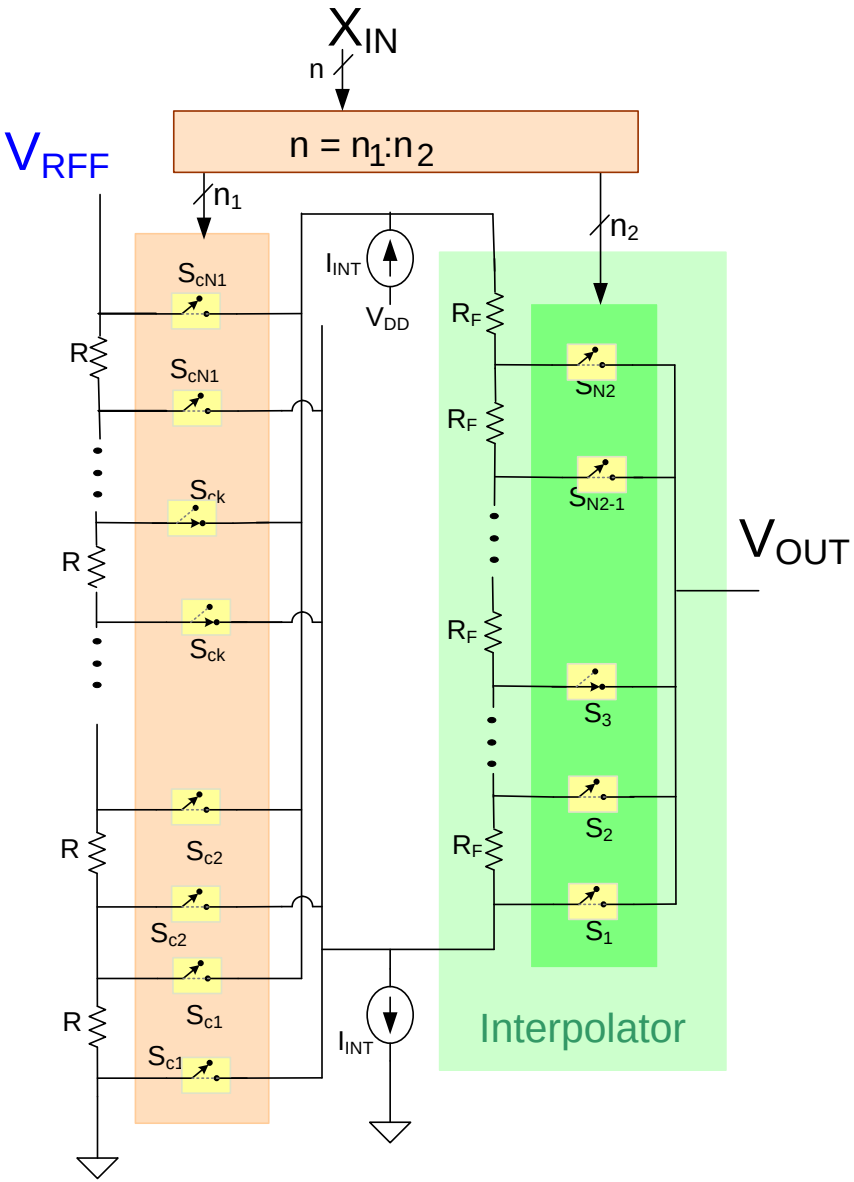
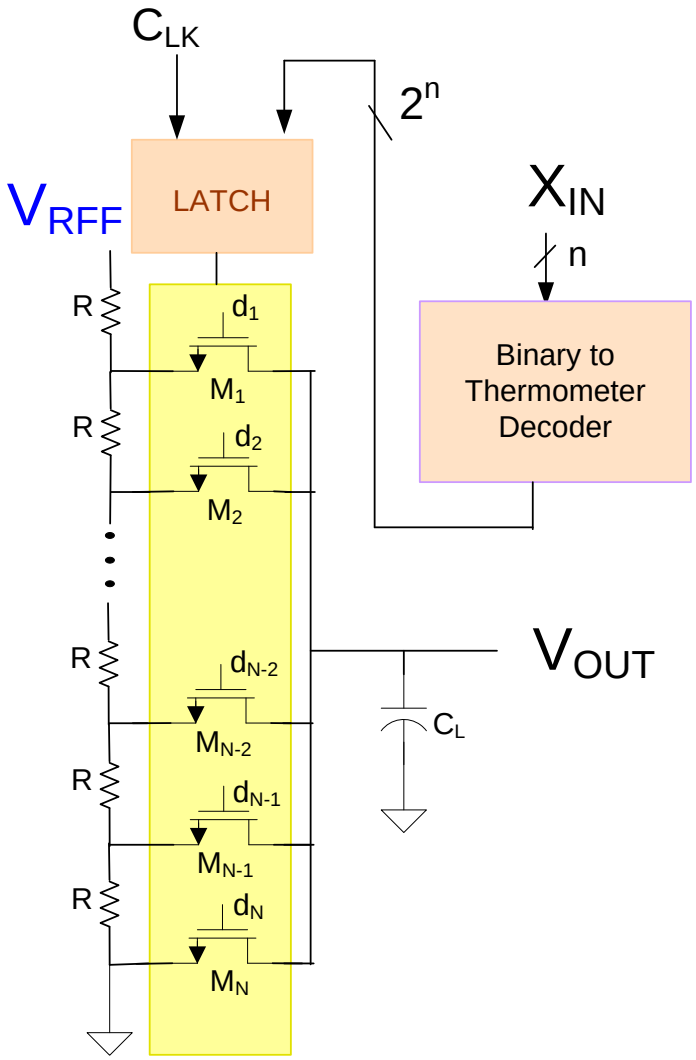
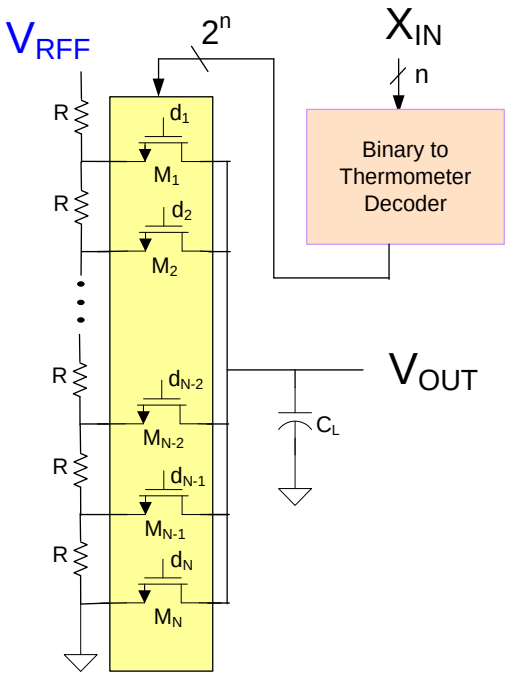
R-String DAC

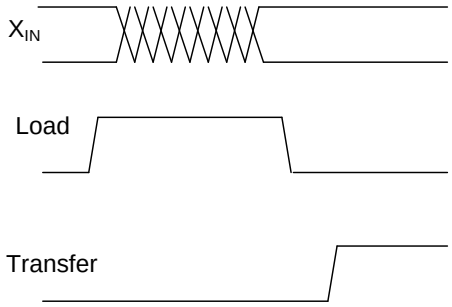
Compensated Fine String Interpolator



Basic R-String DAC



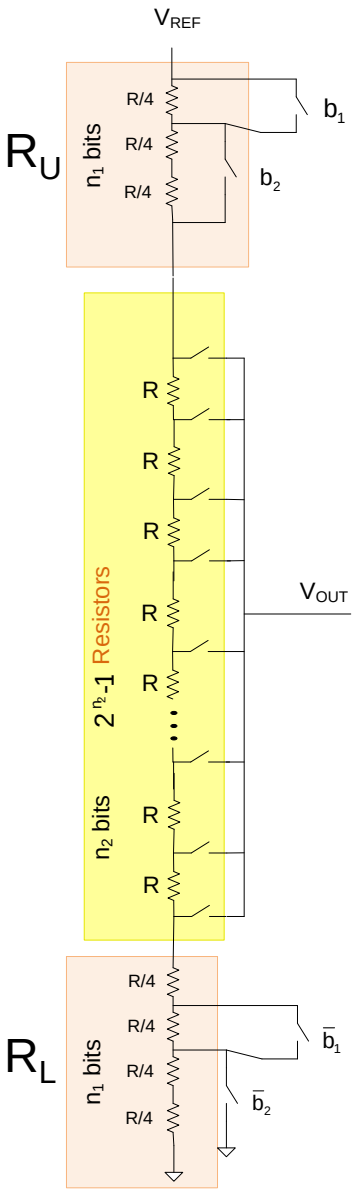




Latching Boolean Signal Can Reduce/Eliminate Logic Transients which Cause Distortion

Basic R-String DAC

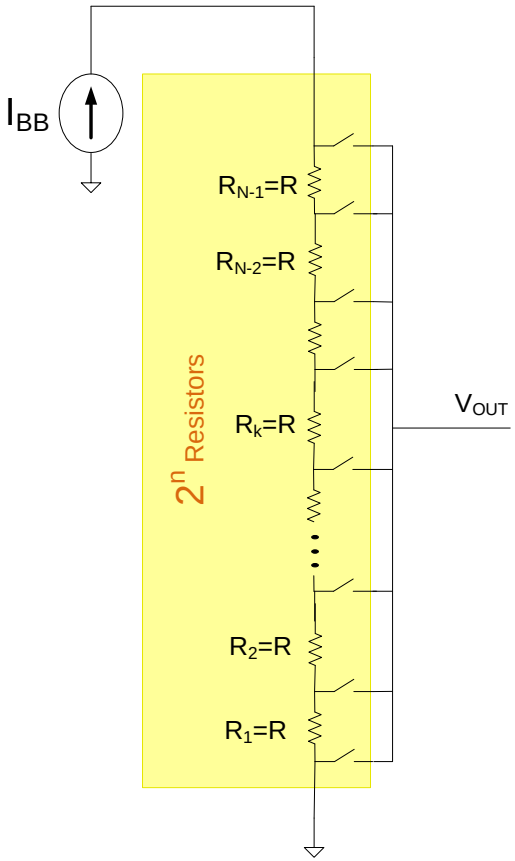
Dither DAC



For all b_1 and b_2, $R_U+R_L=R$

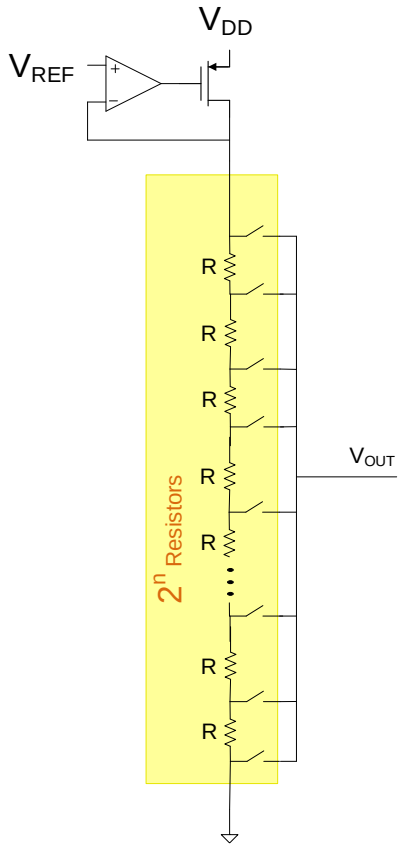
- Another Segmented DAC structure
- Can be viewed as a “dither” DAC
- Often n_1 is smaller than n_2
- Dither can be used in other applications as well

Basic R-String DAC



$$V_{0k} = I_{BB} \bullet \sum_{i=1}^{k} R_k \qquad \text{for } k \geq 1$$

Impedance facing V_{OUT} is code dependent

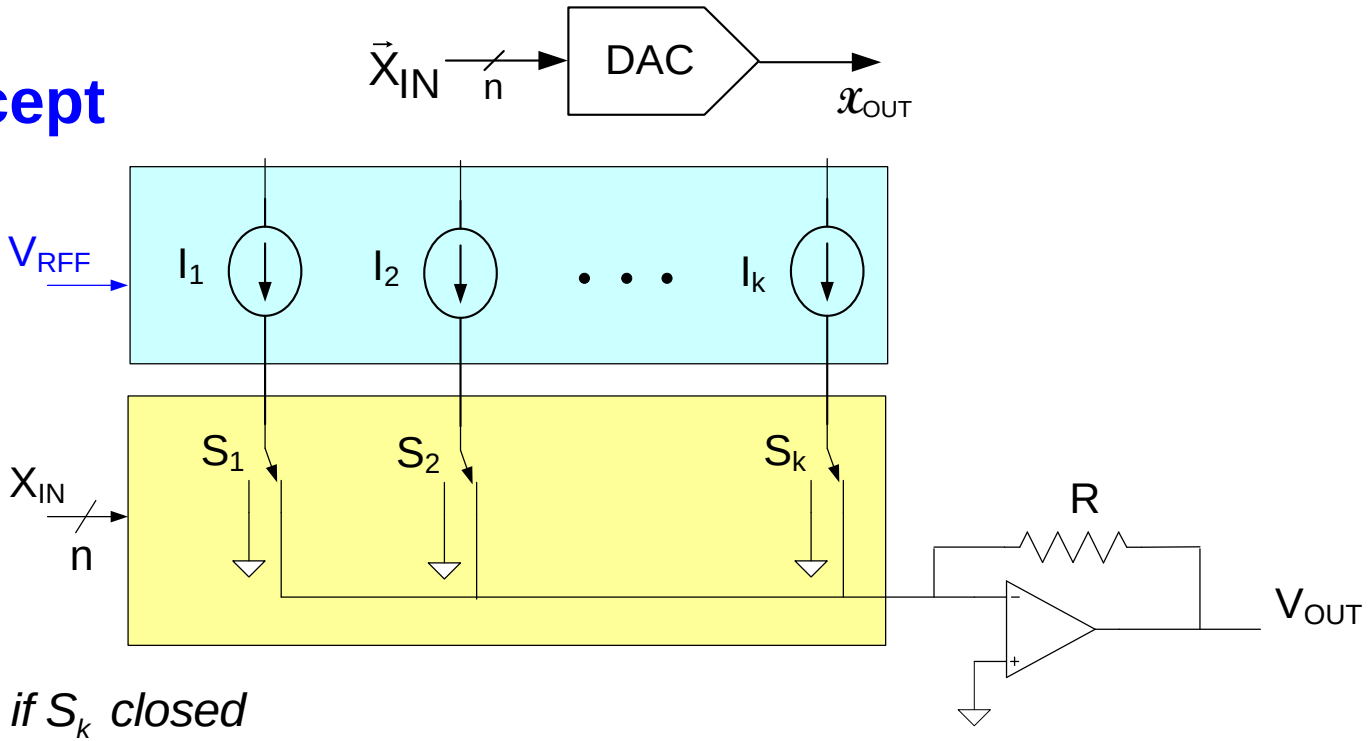


No loading of V_{REF}
Kickback to V_{REF} removed

Current Steering DACs

Current Steering DACs

Concept



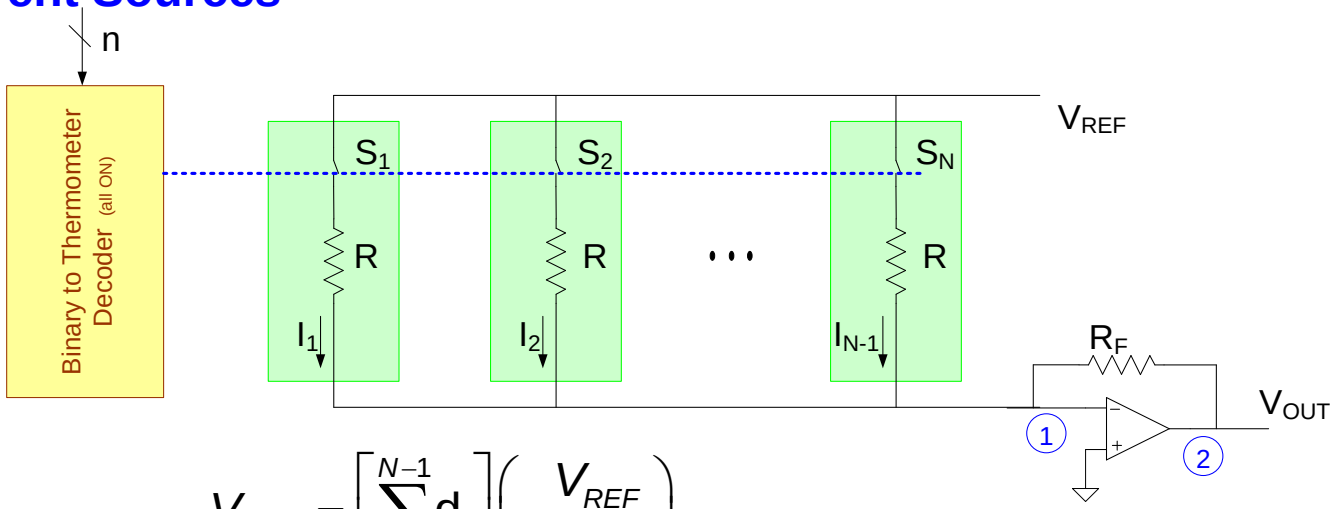
$$d_k = \begin{cases} 1 & \text{if } S_k \text{ closed} \\ 0 & \text{if } S_k \text{ open} \end{cases}$$

$$V_{OUT} = \left[\sum_{I=1}^{k} d_i I_i \right] (-R)$$

- Current sources usually unary or binary-bundled unary
- Termed bottom-plate switching
- Can eliminate resistors from DAC core
- Op Amp and resistor R can be external
- Can use all same type of switches
- Switch impedance not critical nor is switch matching
- Popular MDAC approach

Current Steering DACs

Unary Current Sources



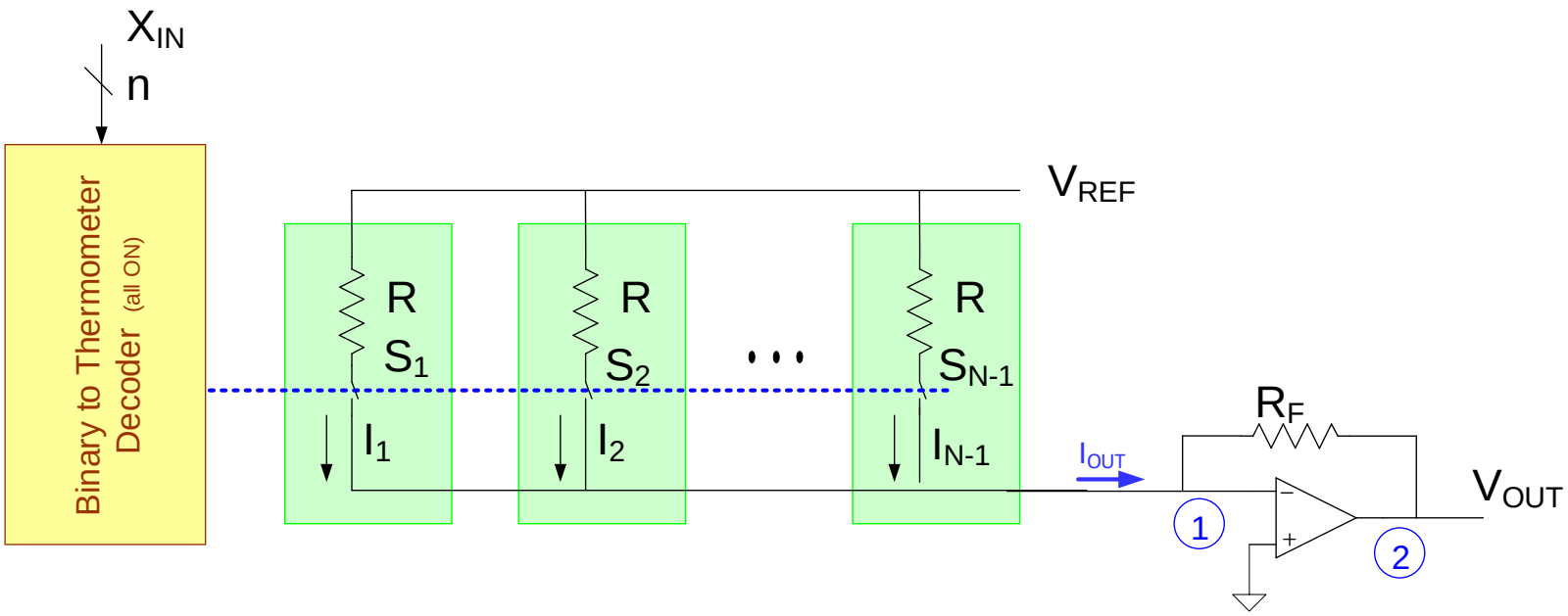
$$V_{OUT} = \left[\sum_{I=1}^{N-1} d_i\right]\left(-\frac{V_{REF}}{R}\right)$$

Inherently Insensitive to Nonlinearities in Switches and Resistors

- Termed “top plate switching”
- Thermometer coding (routing challenge!)
- Excellent DNL properties
- INL may be poor, typically near mid range
- Switch kickback to V_{REF}
- Not suitable for use as MDAC

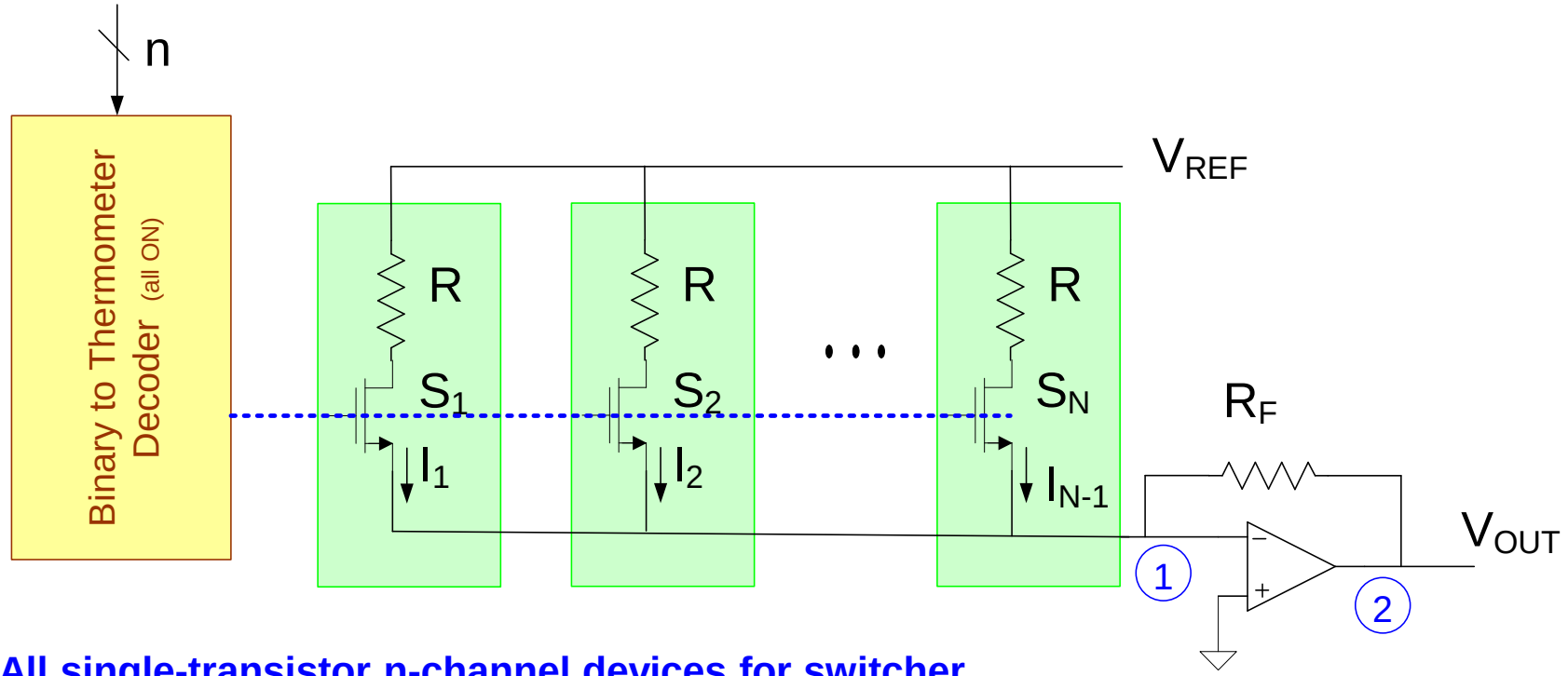
Current Steering DACs

Unary Current Sources



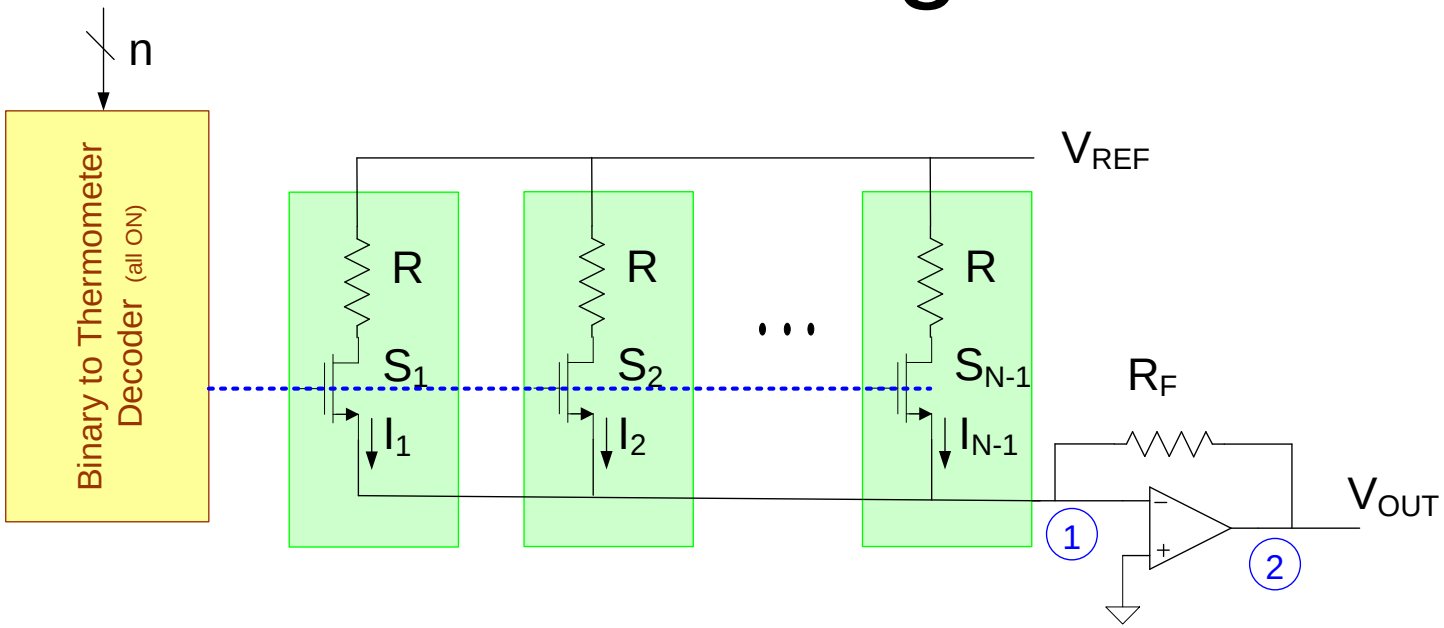
- **Inherently Insensitive to Nonlinearities in Switches and Resistors**
- **Smaller ON resistance and less phase-shift from clock edges**
  - Termed “bottom plate switching”
  - Thermometer coded
  - Can be used as MDAC
  - Reduced kickback to V_{REF}

Current Steering DACs



- **All single-transistor n-channel devices for switcher**
- **Unary R:switch cells**
- **Parasitic capacitances on drain nodes of switches cause transient settling delays**
- **R+Rsw is nonlinear (so nonlinear relationship between I_k and V_{REF}) but does not affect linearity of DAC**
- **Resistor and switch impedance matching important**
- **Previous code dependent transient** (parasitic capacitances on drains of switches)

Current Steering DACs



Transistor Implementation of Switches

$$\beta = \frac{\frac{R_{CELL}}{k}}{\frac{R_{CELL}}{k}+R_F} = \frac{R_{CELL}}{R_{CELL}+kR_F}$$

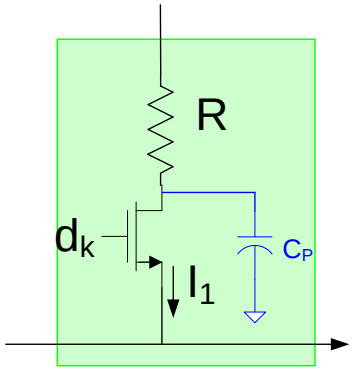
If $V_{OUTFS} = -V_{REF}\frac{N-1}{N}$ $\quad R_{CELL} = \left(\frac{N}{N-1}\right)R_F$

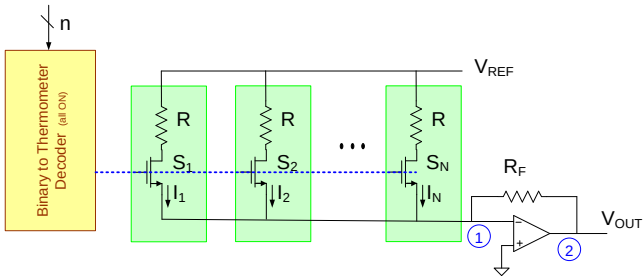
$$\frac{N}{2N-1} < \beta \leq 1 \quad \text{approximately} \quad 0.5 < \beta \leq 1$$

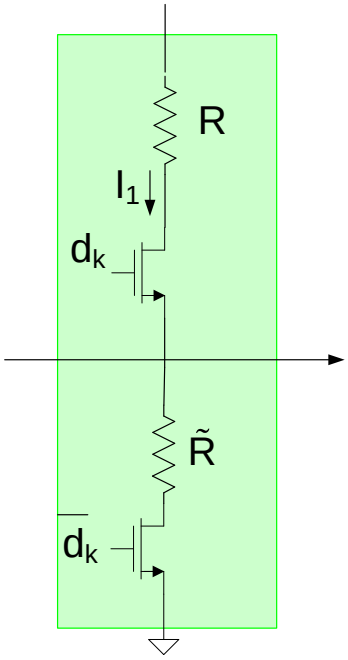
Phase-margin code dependent so distortion will be introduced if not fully settled

Current drawn from V_{REF} changes with code (settling issues if R_{0_VREF} is not 0)

Current Steering DACs



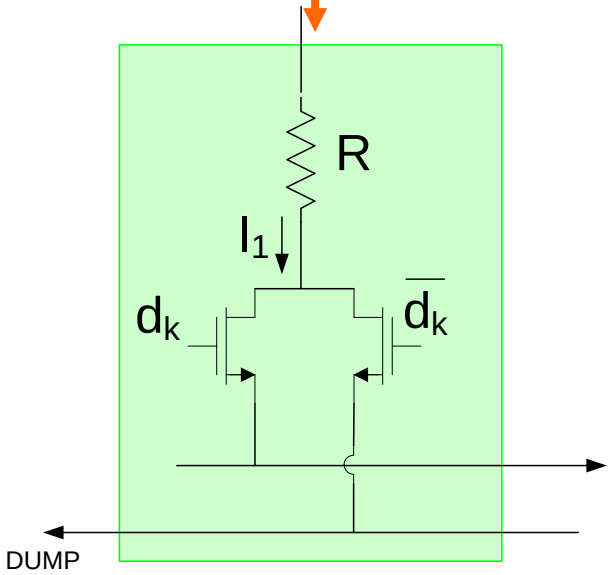




β Compensation

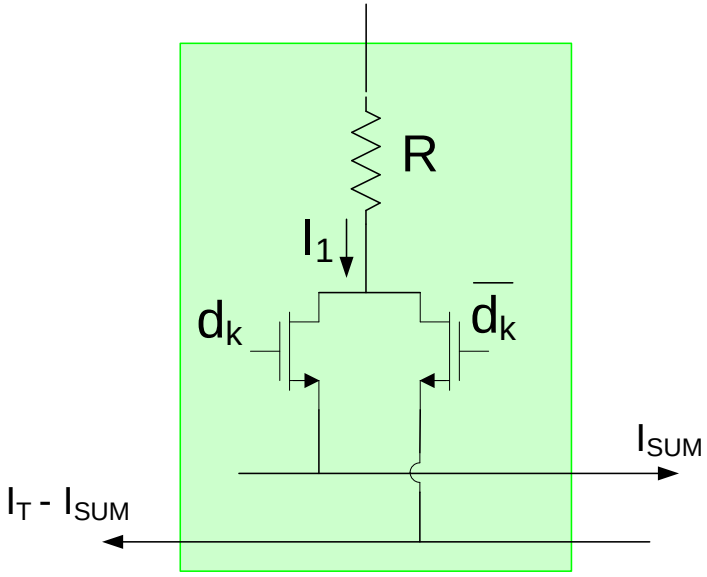
(Actually static β comp)

(keeps β at approximately ½ for all codes, reduces size of compensation capacitor))



C_P Compensation

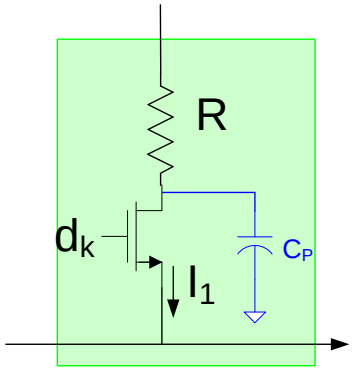
(to keep Cp from charging to V_{REF} when off)

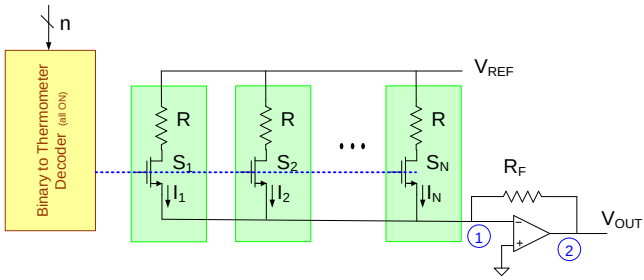


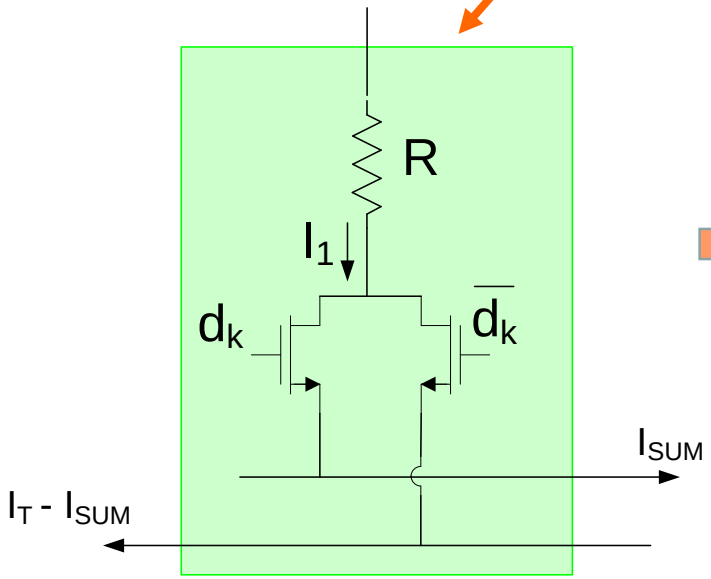
Differential Output

(inherent Cp compensation)

Current Steering DACs



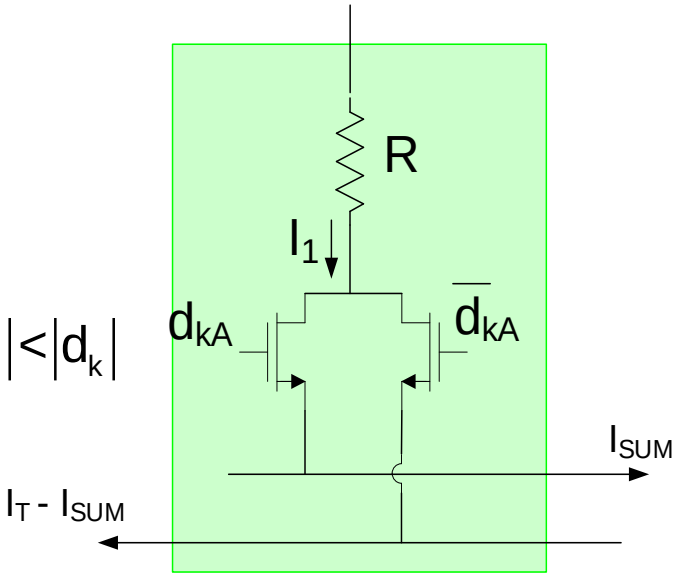




Differential Output

(inherent Cp compensation)

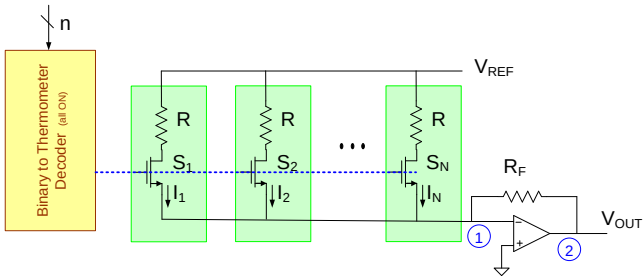
$|d_{kA}| < |d_k|$

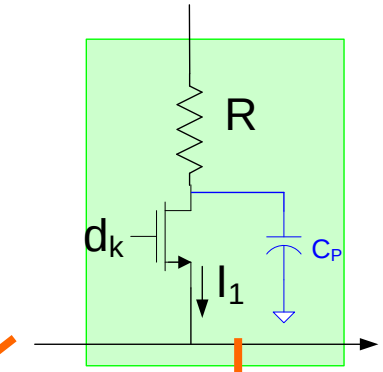


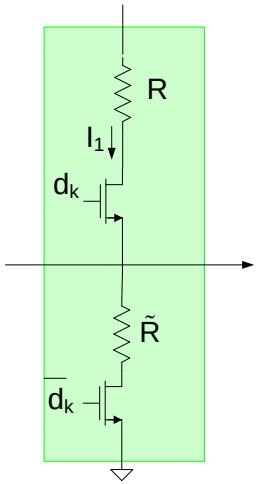
Differential Output

- Steer current rather than switch current
- Signal swing needs to be just large enough to move current from left side to right side

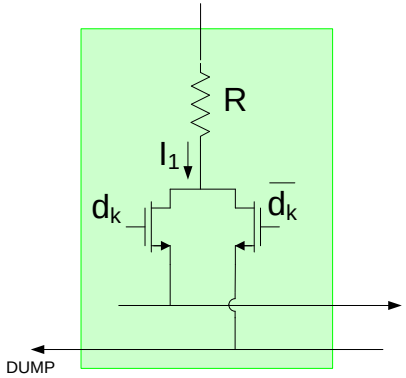
Current Steering DACs



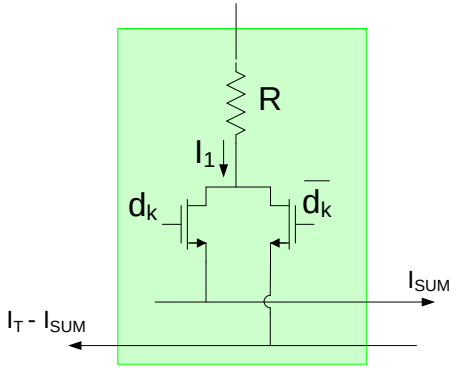




β Compensation



C_P Compensation



Differential Output (switched or steered)

Will β compensation "half" resistance of cells?

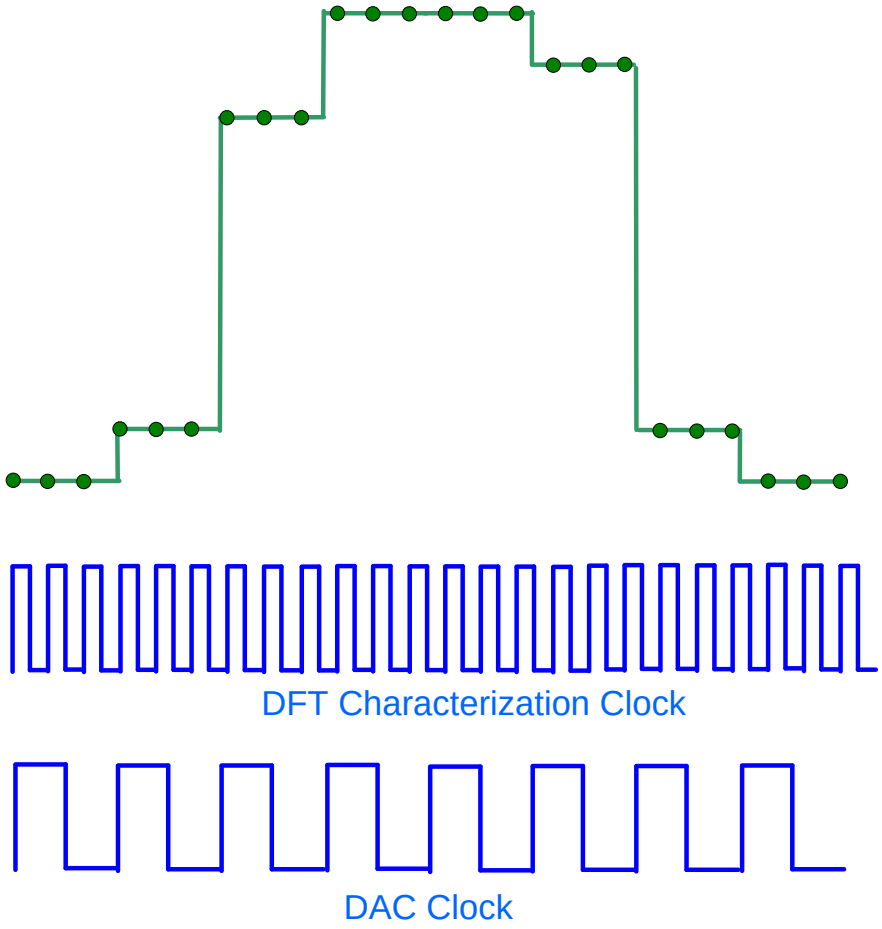
Will β compensation double area for cells?

Is matching of R and compensating R critical?

Can C_p and β compensation be used simultaneously?

Is the frequency-dependent β code dependent?

Spectral Characterization of DACs (a measure of linearity)

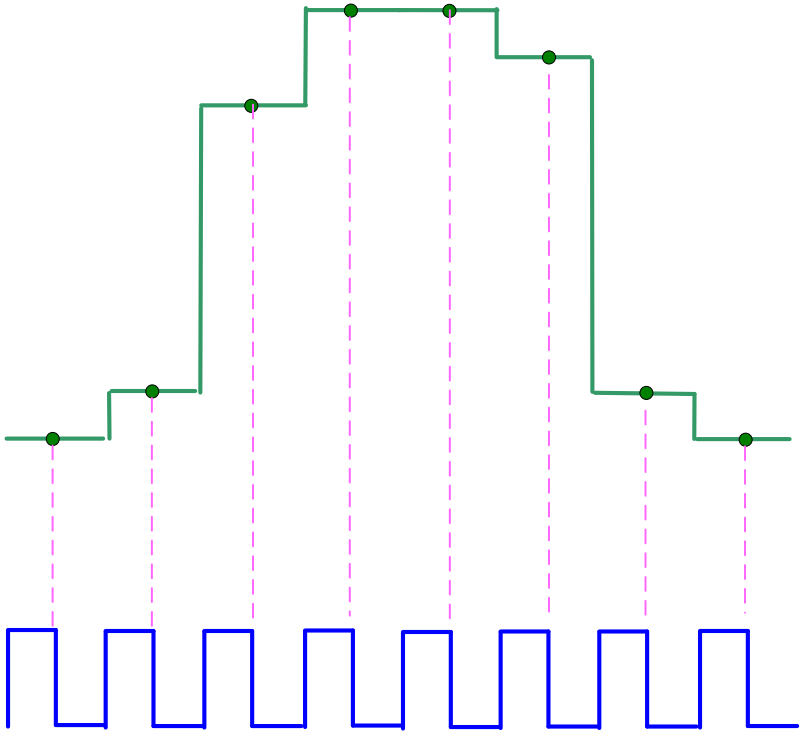


many more samples per DAC clock are often used

(e.g. 64K samples, 31 periods would be approx 2114 samples/period)

Is this how we should characterize the spectral performance of a DAC?

Spectral Characterization of DACs (a measure of linearity)

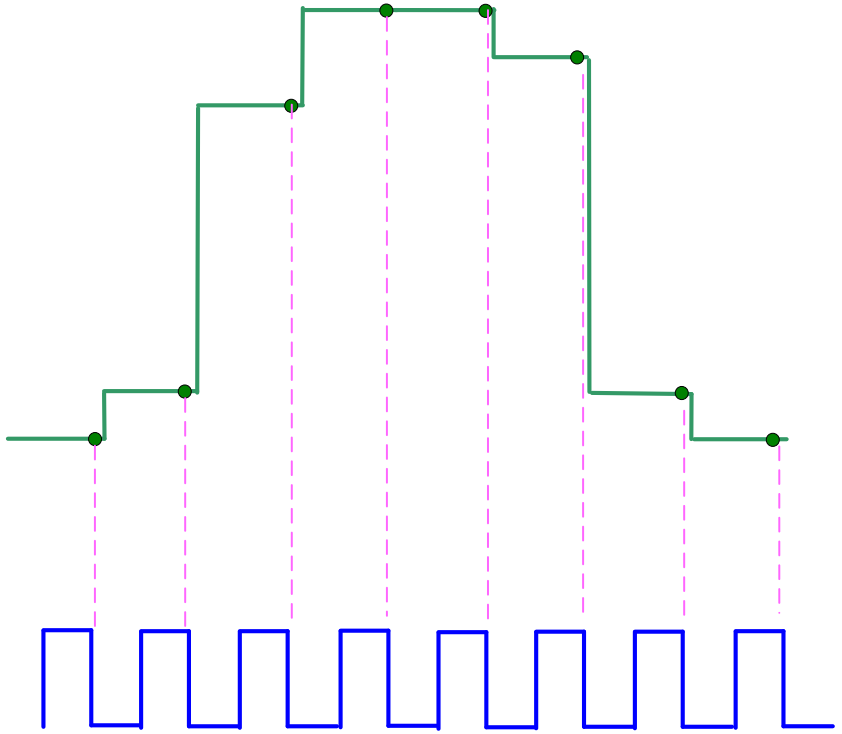


one mid-period sample per DAC clock period (or maybe even less)

Assume Nyquist sampling rate is satisfied

Is this how we should characterize the spectral performance of a DAC?

Spectral Characterization of DACs (a measure of linearity)

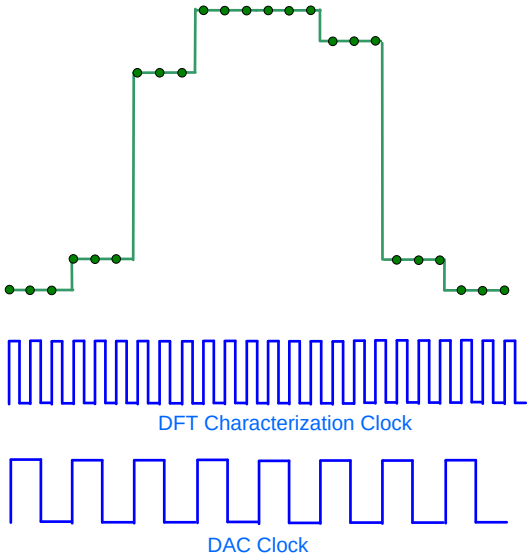


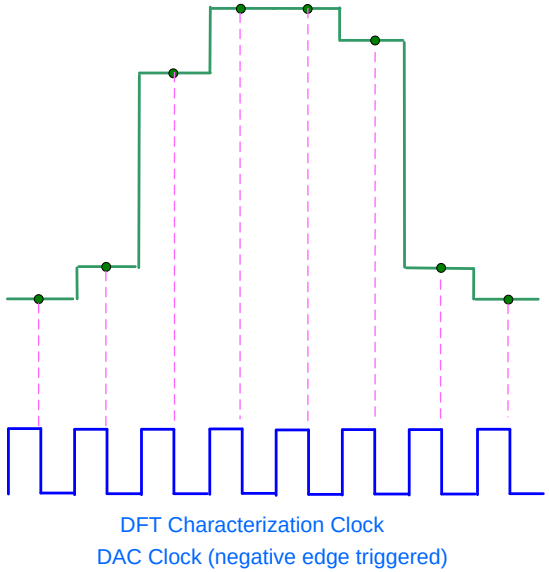
one near-end sample per DAC clock period

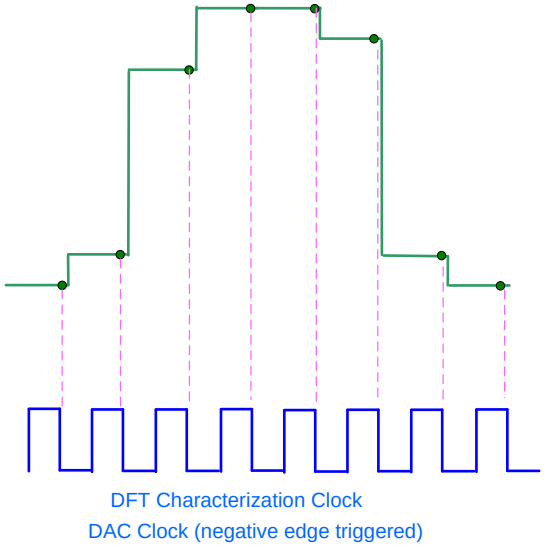
Assume Nyquist sampling rate is satisfied

Is this how we should characterize the spectral performance of a DAC?

Spectral Characterization of DACs (a measure of linearity)







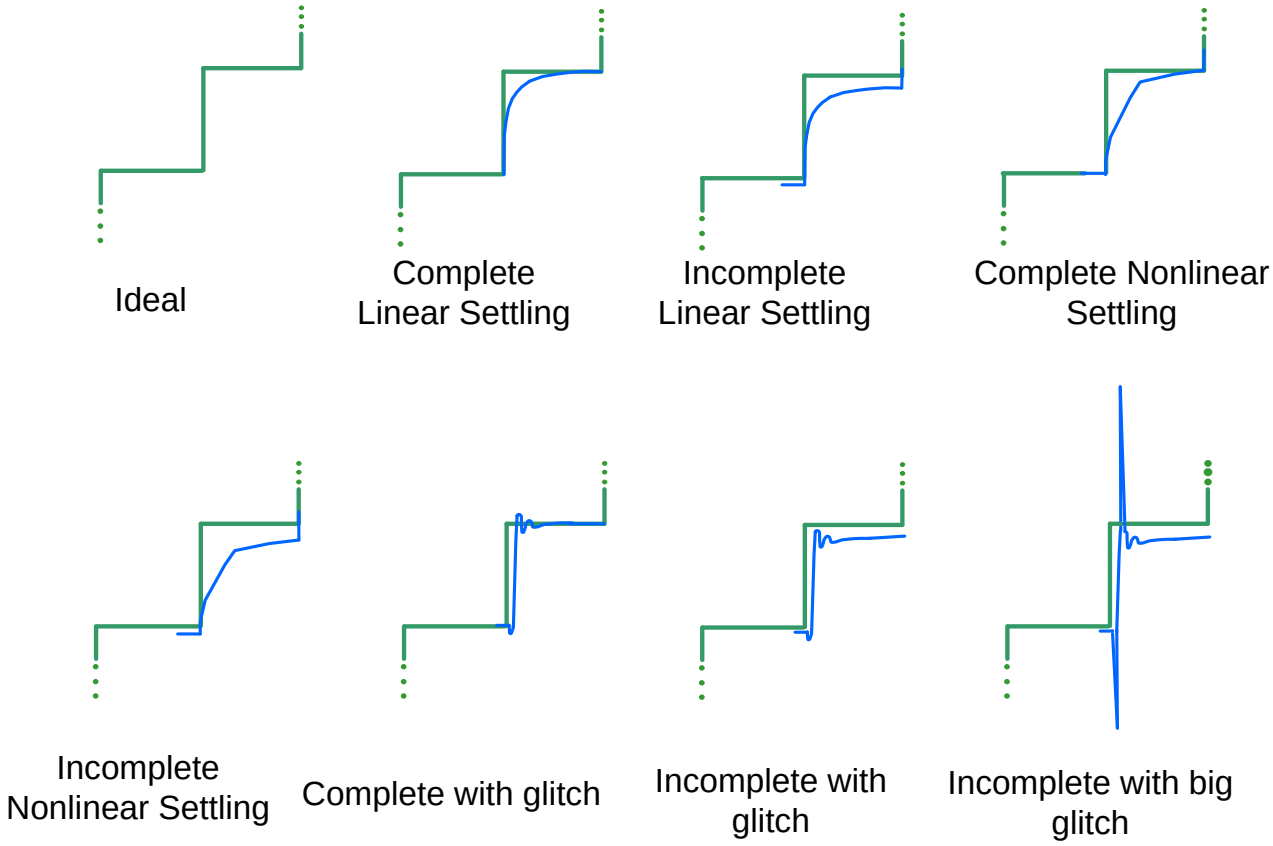
Assume Nyquist sampling rate is satisfied

Does it make a difference?

Yes ! But depends on application which is useful

Spectral Characterization of DACs (a measure of linearity)

Does it make a difference?

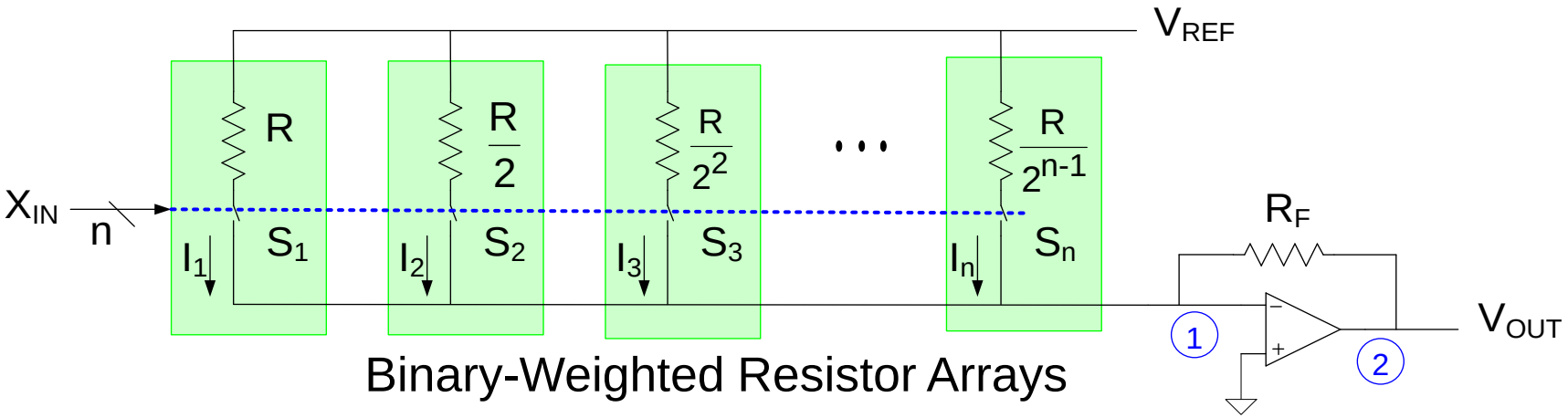


Yes ! But depends on application which is useful

- If entire DAC output is of interest, any nonlinearity including previous code dependence will degrade linearity
- If DAC output is simply sampled, only value at sample point is of concern

Current Steering DACs

Current Steering



Binary-Weighted Resistor Arrays

- Unary cells bundled to implement binary cells (so no net change in number of cells)
- Need for decoder eliminated !
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical
- Large total resistance

Observe thermometer coding and binary weighted both offer some major advantages and some major limitations

Large DNL dominantly occurs at mid-code and due to ALL resistors switching together

Can unary cell bundling be regrouped to reduce DNL

Stay Safe and Stay Healthy !

End of Lecture 15